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ABSTRACT OF THE DISCLOSURE

PROCESSOR AND METHOD OF EXECUTING A LOAD INSTRUCTION THAT BIFURCATE LOAD EXECUTION INTO TWO OPERATIONS

A processor implementing an improved method for executing load instructions includes execution circuitry, a plurality of registers, and instruction processing circuitry. The instruction processing circuitry fetches a load instruction and a preceding instruction that precedes the load instruction in program order, and in response to detecting the load instruction, translates the load instruction into separately executable prefetch and register operations. The execution circuitry performs at least the prefetch operation out-of-order with respect to the preceding instruction to prefetch data into the processor and subsequently separately executes the register operation to place the data into a register specified by the load instruction. embodiment in which the processor is an in-order machine, the register operation is performed in-order with respect to the preceding instruction.